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| 10/525,475 | 02/23/2005 | Hein Otto Folkerts | NL020802US | 7522 |

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| EXAMINER | |
|---|---|
| NADAV, ORI | |

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| 2811 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/525,475 | FOLKERTS ET AL. | |
| | Examiner | Art Unit | |
| | Ori Nadav | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2,3,5-8,13-15 and 20-23* is/are pending in the application.

4a) Of the above claim(s) *8,14 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5-7,13 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2009* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

The amendment filed on 5/13/2009 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: Although the specification describes in the embodiment of figure 8 that the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor, there is no support in the embodiment of figure 4 for the claimed limitation of "the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor".

Applicant is required to cancel the new matter in the reply to this Office Action.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2-3, 5-7, 13 and 20-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the elected embodiment of figure 4 for the claimed limitation of "gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region", as recited in claim 2.

There is no support in the elected embodiment of figure 4 for the claimed limitation of "the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor", as recited in claims 6 and 22.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-3, 5-7, 13 and 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention

The claimed limitation of the surface being provided with a number of cells, as recited in claims 2 and 6, is unclear as to how a two dimensional element (surface) can be provided with three dimensional elements (number of cells).

The claimed limitation of well region extends from the surface into the semiconductor body, as recited in claims 2 and 6, is unclear as to how the well region can extend from the surface into the semiconductor body since the well region is located above the surface of the semiconductor body, as depicted in figures 4b and 4c.

The claimed limitation of "a gate of the reset transistor", as recited in claims 6 and 22, is unclear as to whether said gate in the same element as the "gate region" recited earlier, or a different element.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3, 5, 7, 13, 20-21 and 23, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (6,909,162) in view of Netzer et al. (6,177,293).

Regarding claims 2-3, 5, 7, 13, 20-21 and 23, Wu et al. teach in figure 7 and related text an image sensor comprising:

a semiconductor body 101 having a first conductivity type P and having a surface, the surface being provided with a number of cells,

a cell comprising

a photosensitive element 103 and a reset transistor 121,

the reset transistor comprising

a source region 123, a drain region 125 and a gate region, the source region and the drain region having a second conductivity type N+ opposite to the first, the source

region of the reset transistor being electrically connected to the photosensitive element, wherein

a well region 105 is present which well region extends from the surface into the semiconductor body 101 and extends at least partly below the gate region and the well region having a first conductivity type P,

the source region 123 extending at least substantially in a doped region 103 of the photosensitive element, the doped region having a second conductivity type N, wherein

the source region 123 extends beyond the doped region 103 of the photosensitive element, wherein

the source region 123 extends into the well region 105, wherein

the drain region 125 extends in the well region 105, wherein

the gate is positioned along an edge (the top surface edge) of the photosensitive element, wherein

the source region 123 extends beyond the doped region 103 of the photosensitive element into the well region 105, wherein

the gate region does not extend beyond the well region, wherein

an edge of the gate region extending over the source region is disposed adjacent on an edge of the well region, and wherein

the edge of the well region abuts an edge of the photosensitive element, such that the edge of the gate region is adjacent to the edge of the photosensitive element.

Wu et al. do not teach the gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region.
Netzer et al. teach in figure 2(B) and related text a gate region 227 of a reset transistor 220 overlaps the source region such that a portion of the source region is sandwiched between the gate region and substrate.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region in Wu et al/'s device in order to improve the device characteristics.

Claims 6 and 22, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. in view of Kimura (5,214,683).
Wu et al. teach substantially the entire claimed structure, as applied to claim 1 above except a source follower transistor is present having a gate connected to the source of the reset transistor, the gate of the reset transistor having a length which is longer than the length of the gate of the source follower transistor.
Kimura teaches in figure 1 and related text a source follower transistor 108 is present having a gate connected to the source of the reset transistor 120.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a source follower transistor having a gate connected to the source of the reset transistor, wherein the gate of the reset transistor having a length which is longer than the length of the gate of the source follower transistor, in Wu et al.'s

device, in order to improve the characteristics of the device when using the device in an application which requires a circuit comprising a source follower.

***Response to Arguments***

Applicant argues that there is support for the claimed limitations of "gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region", because "as show in a modified Fig. 4b below, the area within the dashed circle supports the limitation of the gate region (9) overlapping the source region (7) such that a portion of the source region (7) is sandwiched between the gate region (9) and the well region (10)".

The dashed circle shown in modified figure 4b does not provide support for the claimed limitations of "gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region". The dashed circle encloses part of the spacer and the source region, but it is located away from the gate electrode. Figure 4b clearly depicts the gate region not overlapping the source region. Since the gate region does not overlap the source region, then the source region cannot be sandwiched between the gate region and the well region.

Moreover, regarding applicant's argument that "moving the gate as shown by the arrow and described on page 9, lines 8 and 9 increases this overlap of the source (7) by the gate (9)", please note that applicant cannot arbitrarily change the structures of the devices recited in the various embodiments of the present application.

Applicant argues regarding the claimed limitation of "the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor" that "Fig. 13 and page 4 line 14 through page 4 line 22 of the specification supports such a limitation".

If applicant correlates the claimed limitation of "the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor" to the embodiment of figure 4 by introducing new figure 13 and by amending the disclosure in page 4 line 14 through page 4 line 22, then applicant arbitrarily changed the structure of the device of the embodiment of figure 4 in order to fit said claimed limitation to the embodiment of figure 4.

The examiner agrees that the embodiment of figure 8, in paragraph [0073], provides support for the claimed limitation of "the gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor". Thus, applicant can amend figure 8 to illustrate said limitation. However, introducing said limitation into the embodiment of figure 4 constitutes new matter.

Applicant argues that the claimed limitation of the surface being provided with a number of cells, as recited in claims 2 and 6, is clear because "the surface of the semiconductor body is being provided with a number of cells as described in Fig. 1 and page 7 lines 19-30 of the specification. More specifically, the image sensor comprises a number of cells arranged in a two dimensional pattern of horizontal and vertical columns formed along the surface of the semiconductor body".

Figure 1 is merely a schematic diagram of the image sensor and does not clarify how a surface can be provided with a number of cells. Since each cell comprises source, drain and gate regions, each of which is a three dimensional element, it is unclear how a two dimensional element (surface) can be provided with three dimensional elements.

Applicant argues that the claimed limitation of well region extends from the surface into the semiconductor body, as recited in claims 2 and 6, is clear, because "With reference to Fig. 4b, the well region (10) is located below the surface of the semiconductor body (3) and above the semiconductor (2)".

Claims 2 and 6 recite "a semiconductor body having a first conductivity type". Figure 4b clearly depicts element 2, and not element 3, as having a first conductivity type. Therefore, element 2 is the "semiconductor body". As such, the claimed limitation of well region extends from the surface into the semiconductor body, as recited in claims 2 and 6, is unclear, because well region 10 is located above the surface of the semiconductor body 2.

Applicant argues that "Netzer et al. does not discloses a well region and the source region extending into the well region whereby the gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region".

Applicant does not explain why Netzer et al. does not discloses a well region and the source region extending into the well region whereby the gate region overlaps the source region such that a portion of the source region is sandwiched between the gate region and the well region. Netzer et al. clearly teach in figure 2(B) and related text a gate region 227 of a reset transistor 220 overlaps the source region such that a portion of the source region is sandwiched between the gate region and substrate.

Applicant argues that "Kimura does not suggest or teach that the length of the gate of the reset transistor is greater than the length of the source follower transistor. It is respectfully submitted that Kimura does not disclose a gate of the reset transistor having a length which is greater than a length of the gate of the source follower transistor".

Kimura teaches in figure 1 and related text a source follower transistor 108 is present having a gate connected to the source of the reset transistor 120. And, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a source follower transistor having a gate connected to the source of the reset transistor, wherein the gate of the reset transistor having a length which is longer than the length of the gate of the source follower transistor, in Wu et al.'s device, in order to improve the characteristics of the device when using the device in an application which requires a circuit comprising a source follower.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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11/10/2009

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